Growth of Antimony Telluride and Bismuth Selenide Topological Insulator Nanowires

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Topological insulators are a relatively new class of materials, which are insulating in the bulk and conductive on the surface. Surface conductance measurements of topological insulators are often obscured by impurities in the bulk. Nanowires made of a topologically insulating material provide a solution to this problem with their large surface-area-to-volume ratio. I examine the growth procedure for the topological insulator nanowires Sb_2Te_3 and Bi_2Se_3. Growth of antimony telluride nanowires was unsuccessful, but I achieved dense growths of hexagonal microplates. Bismuth selenide nanowires were grown, but it is unclear as to the ratio of bismuth and selenium present. Future experiments include the fabrication of single-nanowire devices and measurement of the conductance.

I. INTRODUCTION

Topological insulators have the unique property of an insulating bulk material while remaining conductive on the surface. This special property of topological insulators is the result of the quantum spin Hall effect.[1] The basis of the quantum spin Hall effect is in the general Hall effect and the quantum Hall effect. The Hall effect describes the phenomenon of an induced voltage in a conductor carrying an electric current in the presence of a perpendicular magnetic field. The quantum Hall effect describes a similar situation in semiconductors at low temperatures and high magnetic fields, but the induced voltage will cause all current to appear on the surface while the bulk appears insulating. In the simplest case, one dimension, the top surface will have current in one direction, while the opposite surface has current moving in the opposite direction. Furthermore, the quantum Hall effect causes a quantization of the material's conductance. The conductance is given by the equation $\sigma = ne^2/h$, where n is an integer.[2] The quantum spin Hall effect differs from the quantum Hall effect in that each surface carries spin in opposite directions.[1] For example, the top surface might carry spin-up electrons to the left and spin-down electrons to the right, while the bottom surface carries spin-up electrons to the right and spin-down electrons to the left. Because of this localization of spin, topological insulators have potential applications in spintronics. Another advantage of the quantum spin Hall effect over the quantum Hall effect is that it does not require a low temperature or a large magnetic field, making it much more useful for applications.

II. METHOD

A. Materials

Si wafer
Si/SiO_2 wafer
Acetone 99.9%
Methanol 99.9%
Te powder
Sb powder
Bi_2Se_3 flakes
Poly-L-lysine
Colloidal gold 20nm

B. Substrate Preparation

The Si or Si/SiO_2 wafer was first cleaned acetone and methanol, alternating several times. Then it was sonicated for 10 minutes, rinsed with deionized water, and dried with N_2 gas. The substrate was coated with poly-L-lysine for 1 minute, then rinsed with deionized water and dried with N_2 gas. The poly-L-lysine gives the surface a net positive charge, which allows the gold nanoparticles to stick to the surface. The substrate is coated with the colloidal gold for 1 minute, then rinsed with deionized water and dried with N_2 gas. Now the surface is coated with gold nanoparticles, which allow the VLS growth of nanowires.

C. Sb_2Te_3

The growth method for Sb_2Te_3 was based on the conditions reported by Lee et al.[3] The precursor Sb and Te powders were placed in a glass tube with the substrate, and were heated to a temperature of 400-500 °C for 2-3 hours in a Lindberg Blue M furnace. N_2 gas was used to carry the precursor vapor down the tube to the substrate at a rate of 80-130 sccm. Ideal locations for each precursor and the substrate are given in Figure 1.

D. Bi_2Se_3

The growth method for Bi_2Se_3 is based on the method reported by Kong et al.[4] The single precursor of Bi_2Se_3 was ground up into a powder and placed in the center of the tube. It was heated to a temperature of 500-550 °C for 2-4 hours, with N_2 gas flowing at a rate of 10-30 sccm. Ideal locations for the substrate

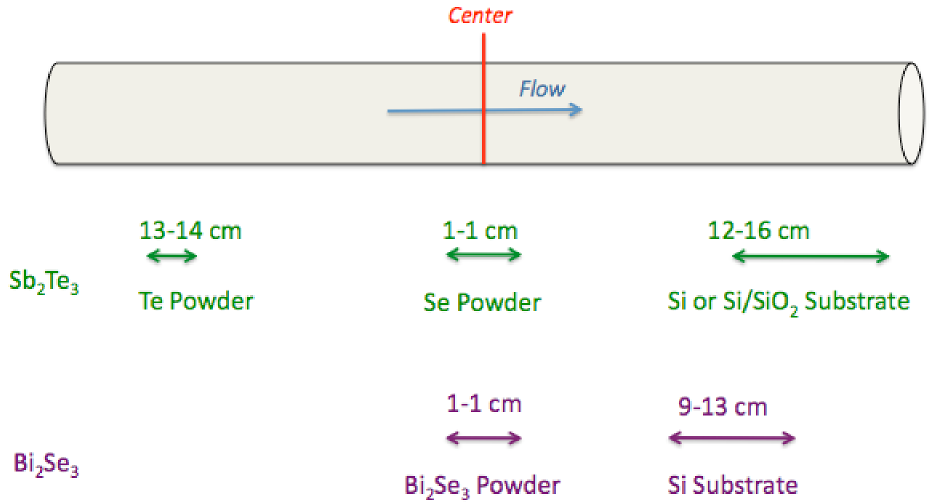

FIG. 1. Ideal precursor and substrate locations.

are shown in Figure 1.

III. RESULTS

A. Sb_2Te_3

I was unable to replicate the nanowire growth described by Lee et al.[3] Most of the growth that occurred was in the form of hexagonal microstructures, as seen in Figure 2. The X-Ray Diffraction data seen in figure 3 shows that the composition of the hexagonal microstructures is unclear, but it is likely a combination of Sb_2Te_3 and SbTe.

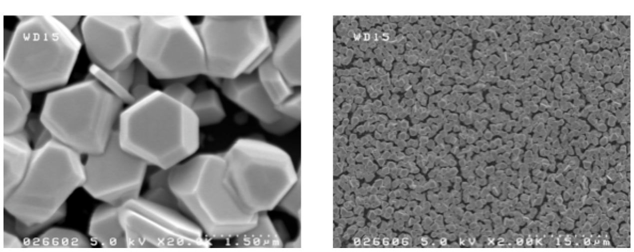

FIG. 2. Hexagonal microstructures of Sb_2Te_3

B. Bi_2Se_3

Sparse nanowire growth was achieved at a temperature of 530 °C, a flow rate of 30 sccm, and a substrate location of 9-13 cm from the center of the oven. The growth included nanowires of various widths, from 30 nm to 500 nm across. Also observed were tapered nanowires, which abruptly changed widths. Various nanowires are shown in Figure 5, while different widths of nanowires can be seen in Figure 7. Figure 6 shows a nanowire with the gold nanoparticle tip, indicating that the growth method is indeed VLS. Lowering the flow rate and moving the substrate to 11-15 cm from the center caused much denser growth with some wires interspersed among dense crystal growth. The X-Ray Diffraction data for this growth shown in figure 4 clearly shows that the composi-

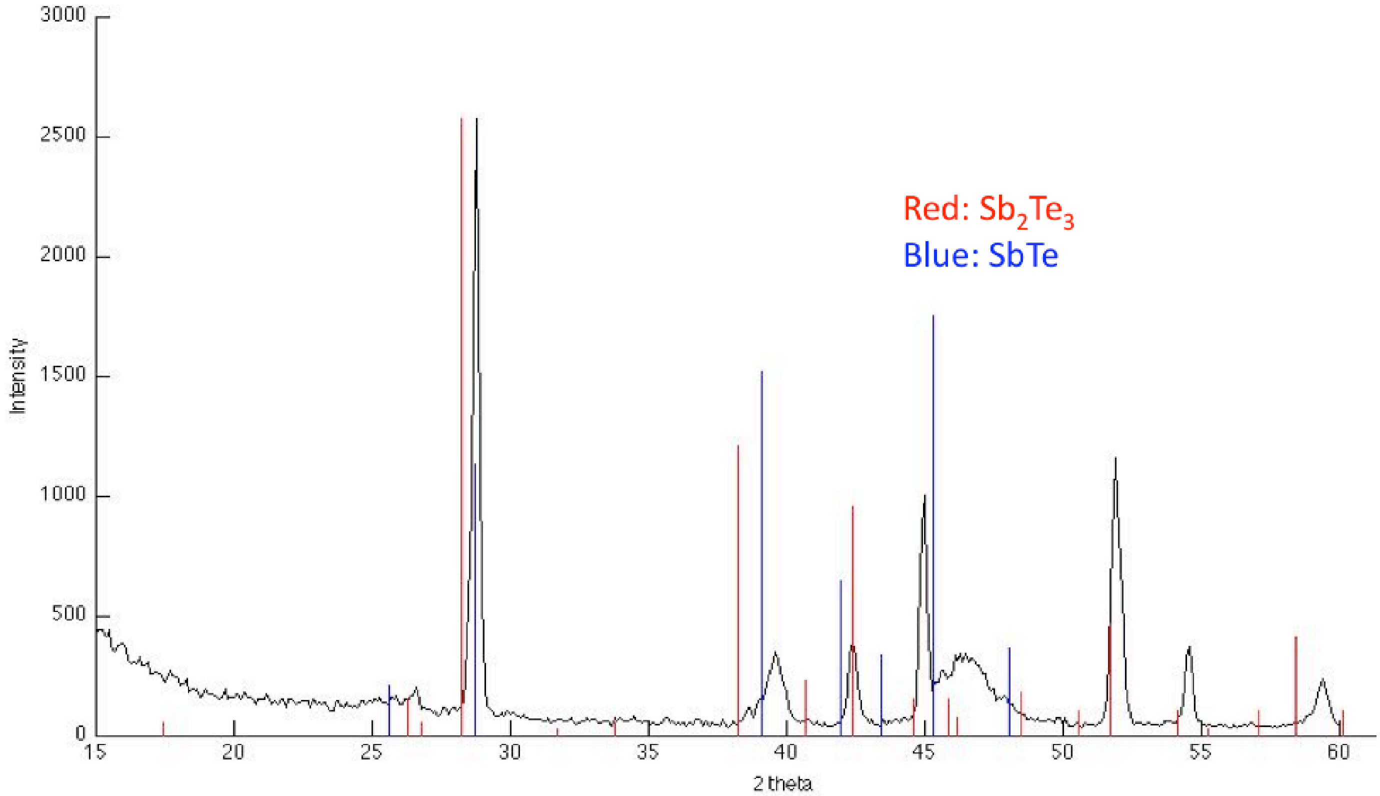

FIG. 3. X-Ray diffraction data for antimony telluride

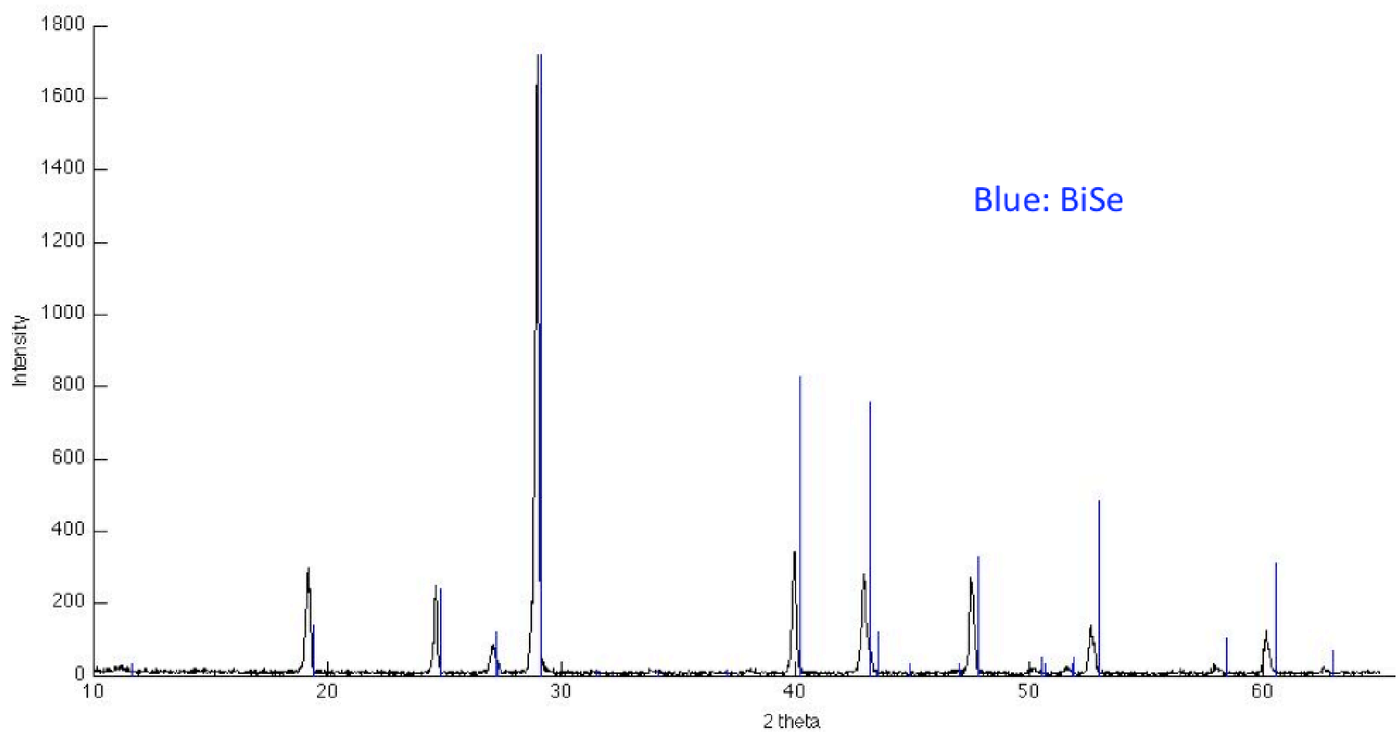

FIG. 4. X-Ray diffraction data for bismuth selenide

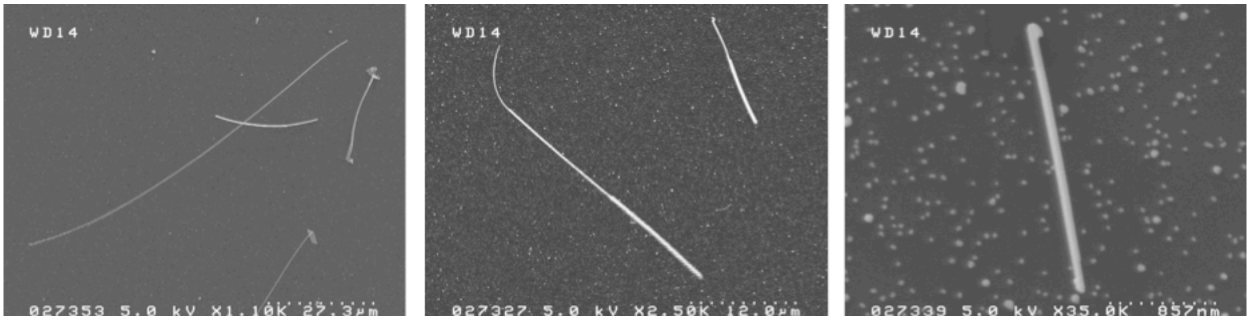

FIG. 5. Various BiSe nanowires

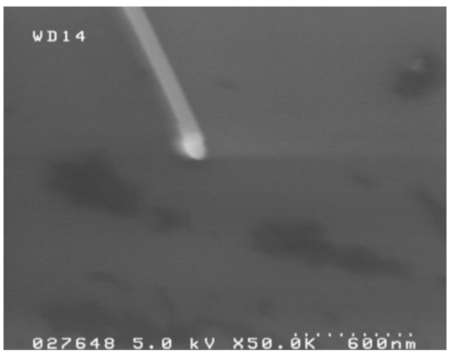

FIG. 6. VLS growth of BiSe nanowire

tion is BiSe; not the expected Bi_2Se_3. It is likely that this is the composition of both the crystals and the nanowires in the sample, as many of the wires grew out of the crystals.

IV. CONCLUSION AND FUTURE WORK

The Sb_2Te_3 growth results of Lee et al. could not be replicated, and while growth of bismuth selenide nanowires was successful, the ratio of elements in the wires is likely 1-to-1. Further experiments could be done to grow Sb_2Te_3 nanowires or to improve the density of growth of bismuth selenide wires. Work could be done to change the ratio of the bismuth selenide wires to the topological insulator variety of Bi_2Se_3. One possible way of doing this includes annealing the wires at a high temperature in selenium vapor for several hours. Another possibility is to include selenium powder in the chamber in addition to the Bi_2Se_3 precursor to account for the apparent loss of selenium. Other future work includes the fabrication of single-nanowire devices, which would allow examination of the conductance of the wires.

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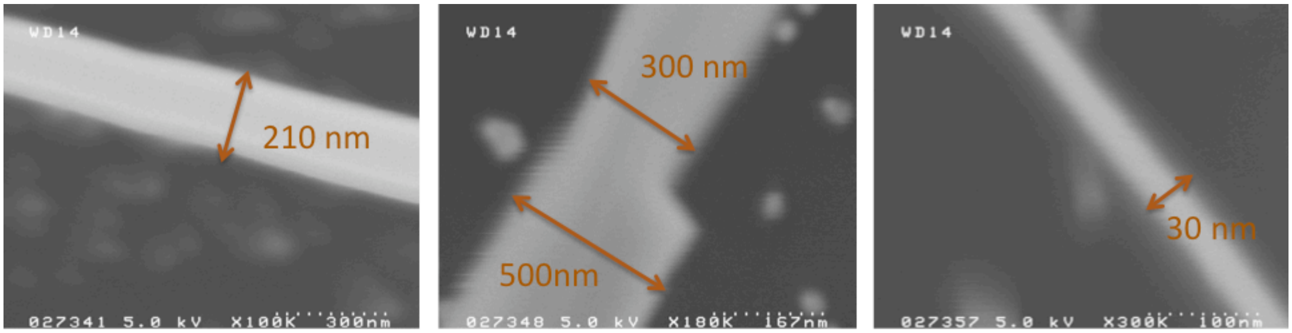

FIG. 7. BiSe nanowires of different widths

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