Characterization of Optical and Electrical Properties in PbSe Quantum Dot Solutions and Thin Films

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Abstract

Over the last decade, high-quality Lead Selenide (PbSe) Quantum Dots (QDs) have been produced via colloidal synthesis [Guyot-Sionnest]. Yu group in UC Davis seeks to better understand the optical and electrical properties of PbSe QDs. My REU project focused on perfecting deposition of smooth QD thin films followed by treatment in hydrazine. Electrical properties of the treated QD thin films were measured by fabricating field effect transistors (FET) and optical properties by infrared spectrum.

Background

When a sample's physical size is smaller than the exciton Bohr radius, quantum confinement effects are displayed; PbSe has a large exciton Bohr radius of 46nm. Colloidal PbSe QDs are usually below 10nm in diameter. Colloidal synthesis of PbSe QDs follows [1]'s growth procedure, and is further discussed in the methods section. This colloidal synthesis method results in PbSe QDs which are capped with organic ligands[2]. The ligands passify[2] the surface of the PbSe QDs. A solution of PbSe QDs in hexane allows for a given sample's optical properties to be measured via Fourier Transform Infrared spectroscopy (FT-IR).

FT-IR measures the absorbance of a sample at many individual wavelengths over a range of wavelengths. Specifically used for this project was the near-infrared spectrum (4000 cm^{-1} to 10,000 cm^{-1}) on a Nicolet 6700 FT-IR with an InGaAs detector. A homebuilt CaF_2 windowed sealed solution device is used to take spectra of PbSe QDs in solution. CaF_2 windows are used because they are very transparent in the desired range. The resulting spectrum from FT-IR yields the first exciton transition by analyzing the lowest energy absorbance peak.

By using the first exciton transition energy from FT-IR measurements, it is possible to determine the average size of the PbSe QDs in a sample. From [3], Equation 1 is a fit that relates the average diameter (between 2-20nm), d_0, of a single PbSe QD and the first exciton transition peak energy, E_0. By solving Equation 1 for d_0, and throwing out the imaginary solution, Equation 2 determines the average diameter of single PbSe QDs from the measured E_0.

The distribution of PbSe QD diameters is proportional to the distribution of the first exciton excitation peak, ΔE, leading to Equation 3. Measuring the ΔE is done by using the Full Width at Half Maximum (FWHM) statistical technique. One method is to fit a Gaussian curve to the first exciton excitation peak yielding the standard deviation, σ. Combining Equation 4 into Equation 3, the percentage size distribution of individual PbSe QDs in a sample is determined by σ and the measured E_0.

Equation 3

$$\frac{\Delta E}{E_0} \propto \frac{\Delta d}{d_0} \tag{3}$$

Equation 4

$$\Delta E = FWHM = 2\sqrt{2\ln(2)}\sigma \tag{4}$$

Equation 5

$$\frac{\Delta d}{d_0} \propto \frac{2\sqrt{2\ln(2)}\sigma}{E_0} \tag{5}$$

A 9:1 hexane octane solution with PbSe QDs is used to deposit a thin film onto a substrate. A small volume, (3-5μL), is large enough to make a thin film about the diameter of a nickel. An ideal thin film is made up of one to several monolayers of PbSe QDs (a single monolayer illustrated in Figure 1). Beginning with Lambert-Beer's Law and using the fit of molar extinction coefficient from [4], the optical density (OD) of a single monolayer of PbSe QDs can be determined

Equation 1: E_0 is in eV and d_0 is in nm

$$E_0 = 0.278 + \frac{1}{0.016{d_0}^2 + 0.209d_0 + 0.45} \tag{1}$$

Equation 2: E_0 is in eV and d_0 is in nm

$$d_0 = \frac{-104{,}500E_0 + \sqrt{3{,}720{,}250{,}000{E_0}^2 + 13{,}931{,}541{,}000E_0 - 4{,}160{,}484{,}199} + 29{,}051}{32(500E_0 - 139)} \tag{2}$$

using Equation 10 and Equation 2. In this paper the length of the capping ligands, l, is assumed to be 0.5nm for untreated PbSe QDs.

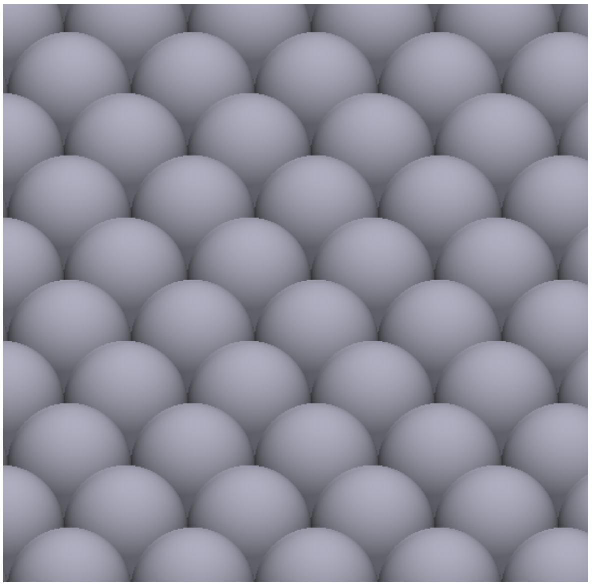

Figure 1: Illustration of an ideal single monolayer superlattice formed by PbSe QDs

Equation 6: Lambert-Beer's Law

$$A = \varepsilon C L \tag{6}$$

Equation 7: Fit of molar extinction coefficient of PbSe QDs in units of $10^5 M^{-1}cm^{-1}$

$$\varepsilon = 0.03389 d_{QD}^{2.53801} \tag{7}$$

Equation 8: Optical Length of PbSe QD; d_{QD} is the diameter of the QD in cm and l is the length of the capping ligands in cm

$$L = d_{QD} + 2l \tag{8}$$

Equation 9: Molar Concentration of PbSe QDs where r_{QD}, d_{QD}, and l are in meters

$$C = \frac{1QD}{V_{QD} N_A} = \frac{1}{\frac{1}{6}\pi \left(d_{QD} + 2l\right)^3 N_A} \tag{9}$$

Equation 10: OD of a single monolayer of PbSe QDs where d_{QD} and l are in nm

$$A = \frac{3.389x10^{20} d_{QD}^{2.53801}}{\frac{1}{6}\pi \left(d_{QD} + 2l\right)^2 N_A} \tag{10}$$

By taking FT-IR absorbance measurements of a thin film sample, the total OD of all monolayers is measured. Simply dividing the measured OD at the first exciton transition peak by the theoretical OD of a single monolayer yields average number of monolayers over the area of the film (Equation 11). The average height of the thin film may then be estimated by multiplying the average number of monolayers by the average diameter of a single QD shown in Equation 12.

Equation 11: Average number of monolayers of the thin film

$$N_{monolayers} = \frac{OD_{peak}}{A} \tag{11}$$

Equation 12: Average height of an untreated thin film of PbSe QDs

$$H_{avg} = N_{monolayers} \left(d_{QD} + 2l\right) \tag{12}$$

A more direct method of determining the height of the thin film is to use AFM, or other high resolution microscopy techniques such as TEM, which verifies the theoretical value in Equation 12.

Some groups have used a thin film of PbSe QDs on a doped-Si SiO_2 wafer to create n- and p-type FET [2]. Briefly, the conductivity between the source and drain of a FET is affected by an applied electrical field through the gate. Depending on the gate voltage, the applied electrical field will either dope the channel with electrons or holes which will change the number of electrons in the conduction bands.

In order to test the gate dependence, we fabricated blank devices with interdigitated electrodes on 300nm thick SiO_2 coated doped-Si wafer using photolithography (an illustration including a blank device is in Figure 6). The distance between each set of electrodes is 10μm which are 30μm tall. The large number of digits is used to increase the conductance and device area for FT-IR studies. Unfortunately, the large area also increases the likelihood for a short between the electrodes. An acceptable blank device requires a current change of less than 1nA over a 20V range between source and drain before the application of the PbSe QD thin film. We note humidity affects the conductance of a blank device as detailed in the next session and cleaning with acetone may reduce the shunt conductance of the imperfect devices (Figure 2).

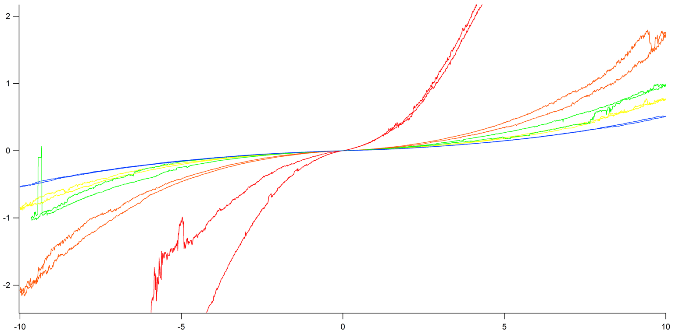

Figure 2: IV curve (μA vs V) of the reduction in conductance as an unacceptable blank device is repeatedly cleaned

After achieving a suitable pre-patterned device, we then deposit a QD thin film on it for FET measurement. Initially, the PbSe QD thin film is quite insulating. This is due to the ligands which cap the surface of the PbSe QDs in the colloidal synthesis [2]. By treating the film with hydrazine, the capping ligands are shortened which increases conductivity substantially [2]. The confirmed model of variable range hopping [2] describes how the reduction in spacing increases conductivity. The hydrazine treatment also injects electrons into PbSe QDs, partially filling the first energy state [2].

Data and Measurements

Optical (FT-IR)

Spectra of both PbSe QDs in hexane solution inside the CaF_2 window solution device and drop-cast thin films on doped-Si wafers with 300nm SiO_2 oxide layer and CaF_2 windows were taken (Figure 3).

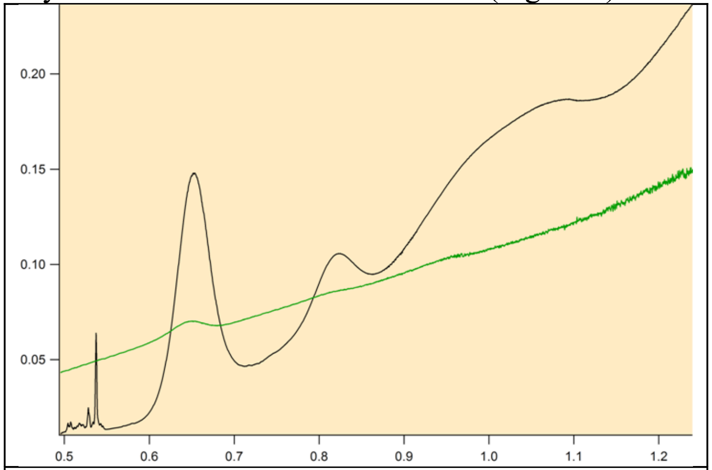

Figure 3: FT-IR OD vs photon energy (eV) for PbSe QDs in hexane solution (black) and thin film on CaF_2 (green) showing first exciton peak

Electrical Measurements

It was discovered that water molecules in the air tended to condense in the 10μm wide channels between the gold electrodes on the blank devices. Before this realization, it was seemingly impossible to get a blank device to have a resistance between the source and drain in the desired 100s of GΩ range—regardless of how clean the area between electrodes appeared under the microscope or even with plasma cleaning. Since then, all electrical measurements on blank and FET devices have been done in a Nitrogen glove box with H_20 concentrations below 0.1ppm. Inside the glove box, a homebuilt probe station is used to apply a voltage to both electrodes of the devices (source and drain) as well a Cu plate to charge the gate. Further explanation on the measurements follows in the methods section. The measurements of the best device, with the highest resistance between the source, drain, and gate, during the REU program is shown in Figure 4 and Figure 5. Figure 4 shows very high resistance between the two electrodes before any film deposition. Figure 5 also shows high resistance between the gate and either electrode, meaning the 300nm thick SiO_2 insulating layer was not ruptured.

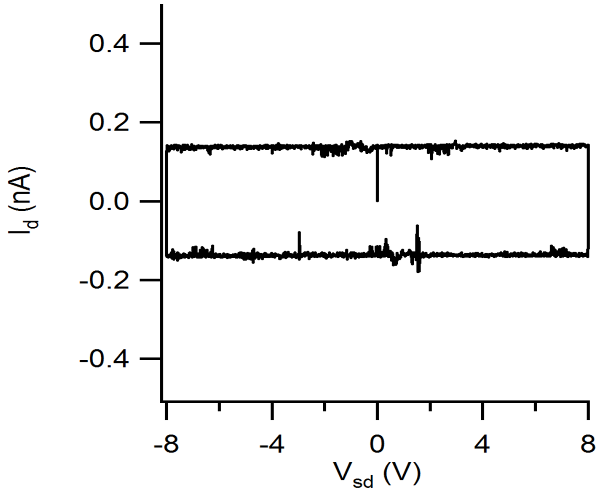

Figure 4: IV curve of current leakage before film between source and drain.

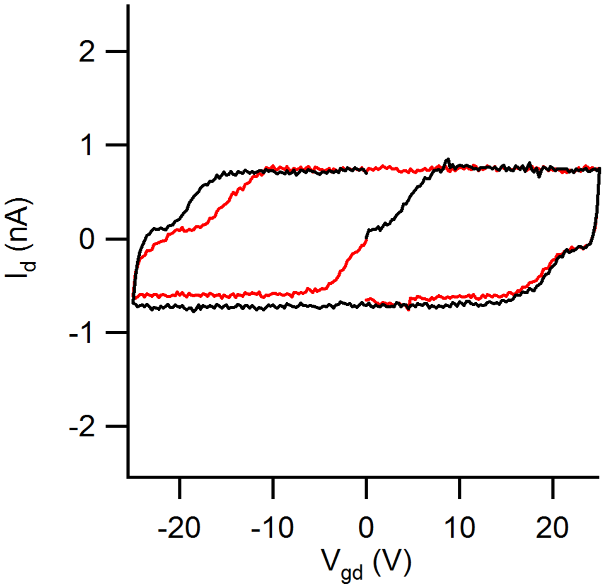

Figure 5: IV curve of gate leakage before film. One electrode is in black, the other is in red.

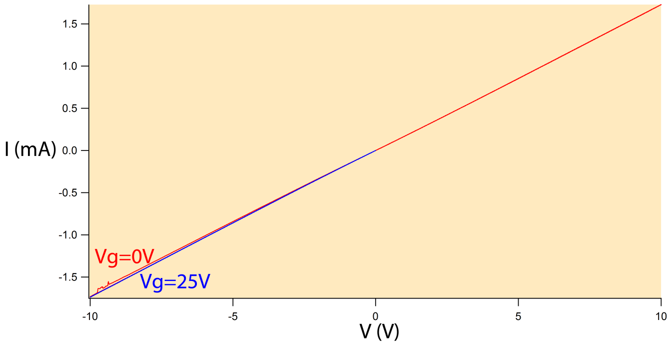

Figure 6: Source-drain IV curve at different gate voltages

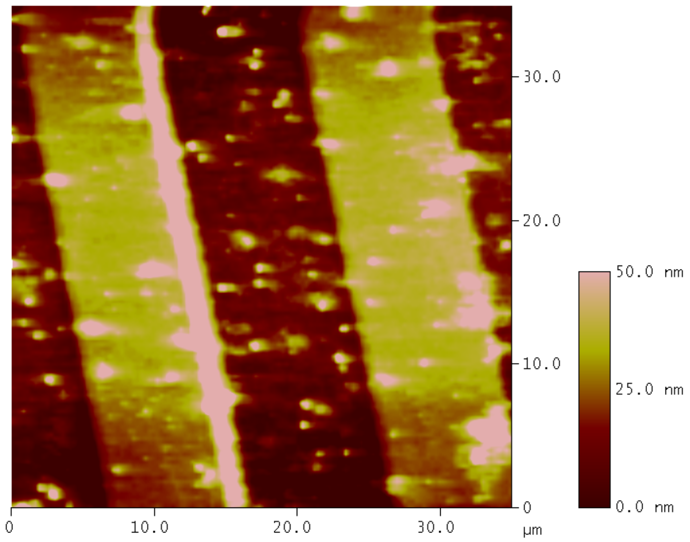

Figure 7: AFM of best device with PbSe QD thin film

Results and Analysis

The initial goal of characterizing the quality of PbSe QD synthesizes was met. Based on FT-IR measurements, the average size and size distribution a PbSe QD synthesis are easily calculated with Equation 2 and Equation 5. The average size of the PbSe QD sample used for all measurements was 6.95nm and had a size distribution of 5.8%. Furthermore, the average number of monolayers in an untreated thin film of PbSe QDs can be calculated from Equation 2 and Equation 11. Using Equation 2, Equation 11, and Equation 12, the height of a given untreated film is estimated.

An additional goal of constructing and measuring a gate dependence on a PbSe QD thin film FET was added during the course of the REU program. A doped-Si wafer with 300nm SiO_2 dielectric insulating layer device was successfully cleaned well within the acceptable parameters (Figure 4); the measurements included becoming comfortable with handling the doped-Si wafer FET devices themselves, the glove box, the probe station inside the glove box, the electrical equipment, and using a homemade LabVIEW program for measuring. After the device was deemed acceptable, a thin film of PbSe QDs was deposited over the entire interdigitated electrode area and measured again. The device was then treated with a 1M hydrazine in acetonitrile solution for 12 hours. As expected, the conductance of the film increased dramatically (Figure 6). Unfortunately, there was no gate dependence seen on the PbSe thin film FET device (Figure 6).

There are several possibilities identified as to why there was no apparent gate dependence. Compared to [2], the device used has a much thicker oxide layer (300nm verses 100nm). The thicker oxide layer reduces the strength of the electrical field that reaches the PbSe QDs. One other discrepancy from [2] is the electrode material itself; this group uses Cr/Au while [2] uses Ti/Au. Furthermore, the film may be too thick; only the bottom few monolayers may be getting doped while the conduction is still dominated by the top non-doped monolayers. Film quality is another possible candidate; clearly the film is not uniform as clumps can be seen in Figure 7. However the most likely possibility seems to be that the hydrazine treatment went on for too long and made the film too heavily doped to show measurable gate dependence.

Future Research

Beyond the 10 week summer REU program, PbSe QD thin film FET devices will continue to be created and tested. The gate dependence will be used to remove the first exciton excitation peak for FT-IR at both room temperature and low temperature (77K). This may lead to evidence of the number of degenerate electron states in the first exciton transition as well as illuminate the charge carrier transport mechanisms; the model of Variable Range Hopping confirmed for PbSe QDs[2]. Another goal of testing the PbSe QD thin film FET devices is to determine the number of electrons that are doped into the crystals as a function of time from the hydrazine treatment. Scrutinizing film quality under the lab's AFM may verify Equation 2 and determine both how the film quality affects gate dependence as well as how the number of monolayers degrades the gate dependence.

Acknowledgements

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Methods

Growth

A colloidal PbSe QD synthesis begins with two three necked vials. Add the following to vial one: 0.65g Lead Acetate, 1.5mL Oleic Acid, 2mL of Phenyl Ether, and 8mL of n-trioctylphosphine (TOP). And add 10mL Phenyl ether to vial two. The oxygen is removed by three purges of three minutes under vacuum followed by two minutes of argon. Once the purging is complete, both vials are heated under vacuum to 75°C for one hour. After heating, put both vials under argon flow, cool vial one to 45°C, and heat vial two to 175°C. Once the two vials are at the correct temperature, inject 1.7mL 1M TOPSe into vial one. Now all of vial one is to be rapidly injected into vial two. For one minute, allow the PbSe QDs to grow in the mixture in vial two. Submerge vial two in a water bath to quickly cool the mixture down—stopping the growth.

Divide the contents of vial two into four centrifuge tubes. Add to vial two 1:1 volume of QD growth solution of hexane and 2:1 volume of QD growth solution of ethanol. Arrange the four tubes in the centrifuge, so the center of mass is balanced, and centrifuge at 17,000g for 5 minutes. Repeat this step 3 times. Once completed, create a solution of hexane with the PbSe QDs stuck to the sides of the tubes. Pipette the solution into a vial and dry under vacuum for at least 30 minutes.

Materials

Lead Acetate
Oleic Acid
Phenyl Ether
n-trioctylphosphine (TOP)
1M TOP-Se
Ethanol
Hexane
Octane
Hydrazine
Acetonitrile

FT-IR of PbSe QDs in Solution

Clean the CaF_2 windows (very carefully – CaF_2 is extremely brittle), the interior volume of the solution device, and the Teflon pegs with acetone and methanol followed by blowing the residual methanol off with the nitrogen gun. Fill the volume of the solution device with hexane (about 1mL) so there is no large air bubble. Seal the solution device with the Teflon pegs and carefully slide the solution device in the FT-IR sample area. Take a background of hexane in the solution device in Omnic. Remove the solution device from the FT-IR and remove the hexane inside with a syringe. Carefully clean the solution device with acetone and methanol again. Mix about 1.5 mL of hexane with the sample of PbSe QDs and inject the solution into the solution device. Seal the solution device with the Teflon pegs, carefully slide the solution device into the FT-IR sample area, and take a sample in Omnic (with hexane background).

Cleaning a FET device wafer

Several methods were used to clean the FET devices before applying a thin film of PbSe QDs. The basic method to clean the devices is to rinse the interdigitated electrode side with acetone followed by a rinse in methanol and finally blown dry with the nitrogen gun. The purpose of the nitrogen gun drying is to literally blow off all the methanol rather than allowing it to evaporate and leave residue on the device. When drying with the nitrogen gun, the device should be angled nearly vertical with the floor and the nitrogen flow can be thought of as a squeegee: begin at the top of the device and move from side to side while slowing moving toward the bottom of the device. This basic cleaning method is used for removing small shards of Si and SiO_2 after cleaving, before testing a device, and before and after any of the other cleaning methods.

Drop-Cast PbSe QD Thin Film

PbSe QD thin films are produced by dropping PbSe QDs in a solution on to a substrate and allowing the solvents to evaporate; single to several monolayer films are possible with this method. The best film quality was found by preparing a solution of 9 parts Hexane and 1 part octane. Add 0.3mL of the hexane octane solution to the PbSe QD sample and gently mix for several seconds. Using the micropipette, extract somewhere around 3.5-5μL of hexane octane PbSe QD solution. The substrate should be inside of the glove box. Carefully and quickly empty the contents of the micropipette onto the substrate at desired center of the film. Allow at least one minute for the film to dry.

FT-IR of PbSe QD Thin Film

Prepare a background in Omnic of the same substrate used to deposit the film—ideally the substrate used to deposit the film on to. After the film is deposited on the substrate take a sample in Omnic.

Measuring Source-Drain Current

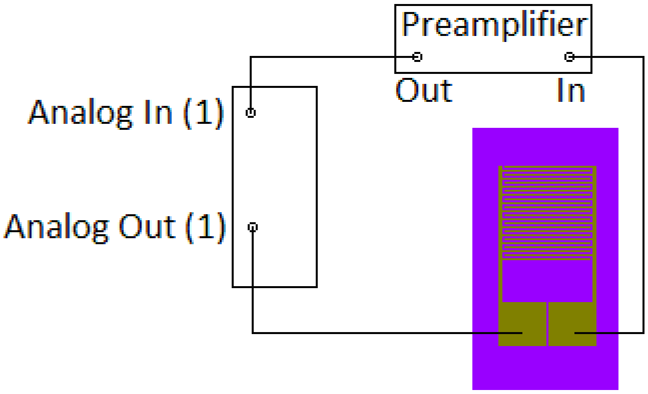

Figure 8: Diagram of wiring to measure source-drain current

Inside the glovebox, carefully place the probes on the large electrode pads— it is very easy to penetrate the 30nm of Au and 300nm of SiO_2 insulating layer to short the gate. Connect the source to Analog Out (1), the drain to the preamplifier's input port, and the preamplifier's output port to Analog In (1) as shown in Figure 8.

Start the MeSuX LabVIEW program, load the standard settings, and adjust the back panel for the desired current level. Click 'Start' on the log and turn the plot on to see the data graphically. Scan the source-drain voltage as desired.

Measuring Gate Leakage and Dependence

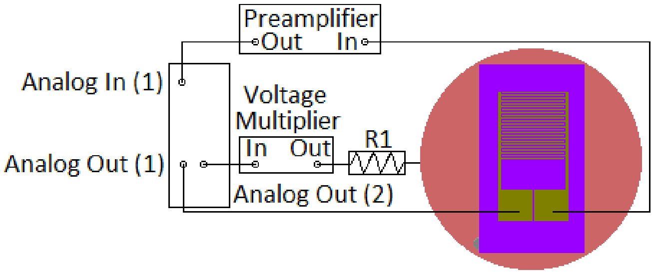

Figure 9: Diagram of wiring scheme to measure source-drain current and charge the gate

Cleave or chip off the oxide layer on the side of the device in order to expose the doped-Si layer. Quickly move the device inside the glove box and place the device on the probe station's Cu plate. Apply a small amount of silver paint to the exposed doped-Si layer to electrically connect the gate to the copper plate. Connect Analog Out (2) to the voltage multiplier's input and the output to the bottom plate through a resistor as shown in Figure 8. Connect the gate and source in the same fashion as in the above section *Measuring Source-Drain Current*. Follow the instructions in the same section for setting up MeSuX. Be sure to verify the correct voltage multiplier is set up in the back panel for Analog Out (2), which controls the gate voltage.

Before attempting to make drain-source measurements with the gate charged, oxide layer must not be broken down. To verify that the dielectric is not broken down, connect one probe to the large pad (and only one—there is a feedback issue if both are connected at the same time) and to the preamplifier's input port. Vary the gate voltage (slowly) and take the IV curve just like measuring source-drain for the two electrodes. Do this for both electrodes and make sure it is at least in the 100's of GΩ range.

To check the gate dependence, change the gate voltage (slowly) and take source-drain measurements in the same way described in the above section. Vary the gate and repeatedly take source-drain measurements to see the gate dependence.